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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,232	01/20/2004	Moon-Kee Chung	45927	6450

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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,232	CHUNG ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/9/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 4, line 17 contains a misspelling of the word "where."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 5 and 12 recite, "classifying the bit strings configuring the read data..." Examiner interprets the "bit strings configuring the read data" as the bit strings which contain the information regarding the shift direction and number of bits to be shifted. Claims 5 and 12 claim to reverse the order of the more and least significant bits of the said bit strings. Examiner notes that in paragraph 30 this operation is explained for carrying out on the read data from a first storage medium, rather than the said bit strings contained within a control register. For this reason, Examiner must reject claim 5 and claim 12 under 35 U.S.C. 112, first paragraph.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1- 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al.

With regard to claim 1, Tokumaru teaches a method for reading and storing data by means of a direct memory access (DMA) medium (Figure 4), comprising the steps of:

Deciding a shift direction and a predetermined number of bits to be shifted in advance (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) when a request is made so that data read from a first storage medium (where a first storage medium may be interpreted as a first memory; column 3, lines 23 – 29) can be processed;

Shifting the bit strings by the predetermined number of bits in the decided shift direction, and transferring the shifted bit strings to a second storage medium (where a second storage medium may be interpreted as a destination memory; column 3, lines 23 – 29; column 2, lines 45 – 56).

Tokumaru fails to teach sequentially storing bit strings configuring the read data in a register.

Staplin et al. teach sequentially storing bit strings configuring the read data (specifically, the shift direction and number of shifts) in a register (interpreted as an F-register; Figure 3, item 51; column 9, lines 18 – 24; Table 1).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to store the shift configuring data as taught by Tokumaru into a register as taught by Staplin et al. This would have been obvious in order to store the configuration values, thereby making it unnecessary to re-compute them in the case where an identical operation is performed twice in a row, thus, making the DMA operation more efficient.

With regard to claim 2, Staplin et al. teach the additional limitation wherein each of the bit strings configuring the read data is configured by one of an 8-bit string, a 16-bit string, or a 32-bit string (column 12, lines 12 – 13).

With regard to claim 3, Staplin et al. teach the additional limitation wherein the number of bits to be shifted has a value from 0 to 7 (column 9, lines 50 – 55; Staplin et al. teach that 4 bits (bits 12 – 15) are used when bit 8 equals a binary 0 to determine the number of positions to be shifted. 4 bits would provide a range from 0 to 15).

With regard to claim 4, Tokumaru teaches the additional limitation wherein the step of deciding the shift direction and the number of bits to be shifted depends upon bit values set by the DMA medium (Examiner interprets the shifting signals, which

determine the shift direction and number of bits (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) as being part of the DNA medium, and therefore the reference meets this limitation).

* * *

Examiner assumes that the applicant meant to recite classifying the read data, instead of classifying the bit strings configuring the read data in the following:

Claims 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al., and further in view of Beukema et al.

With regard to claim 5, Tokumaru and Staplin et al. teach writing the read data to the second storage medium, but fail to teach classifying the bit strings configuring the read data into more significant bit strings and less significant bit strings; and rearranging positions of less and more significant bit strings.

Beukema et al. teach classifying bit strings into more significant bit strings and less significant bit strings and rearranging positions of less and more significant bit strings (Figure 6B, 7B, 8; where classifying bit strings and rearranging positions may be interpreted as reflection; column 9, lines 41 – 60; column 16, lines 60 – 67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the method of Beukema into the method of Tokumaru and Staplin et al. This would have been obvious in order to provide DMA transfers on "mixed endian computing systems" in order to promote better performance

when converting between the two types of data organization (column 2, lines 38 – 43; column 3, lines 51 – 56).

With regard to claim 6, Beukema et al. teach the additional limitation of wherein the read data is configured in the form of 32 bits at the step of rearranging the positions of the less and more significant bit strings (Figure 4C; column 5, lines 52).

With regard to claim 7, Beukema et al. teach the additional limitation of wherein the step of rearranging the positions of the less and more significant bit strings depends upon bit values set by the DMA medium (where a bit value may be interpreted as a "reflection bit" (RB); column 9, lines 41 – 58).

* * *

Claims 8 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al.

With regard to claim 8, Tokumaru teaches an apparatus for reading and storing data by means of a director memory access (DMA) medium (Figure 4), comprising:

A first storage medium for storing data read in a source address (where a first storage medium may be interpreted as a first memory; column 3, lines 23 – 29) ;

The DMA medium for decoding a shift direction and a predetermined number of bits to be shifted in advance when a request is made so that the read data can be

processed, sequentially storing bit strings configuring the read data, shifting the bit strings by the predetermined number of bits in the decided shift direction, and transferring the shifted bit strings (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22);

A second storage medium for storing data transferred from the DMA medium (where a second storage medium may be interpreted as a destination memory; column 3, lines 23 – 29; column 2, lines 45 – 56).

Tokumaru fails to teach sequentially storing bit strings configuring the read data in a register.

Staplin et al. teach sequentially storing bit strings configuring the read data (specifically, the shift direction and number of shifts) in a register (interpreted as an F-register; Figure 3, item 51; column 9, lines 18 – 24; Table 1).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to store the shift configuring data as taught by Tokumaru into a register as taught by Staplin et al. This would have been obvious in order to store the configuration values, thereby making it unnecessary to re-compute them in the case where an identical operation is performed twice in a row, thus, making the DMA operation more efficient.

With regard to claim 9, Staplin et al. teach the additional limitation wherein the DMA medium reads each of the bit strings configuring the data with one of an 8-bit string, a 16-bit string, or a 32-bit string (column 12, lines 12 – 13).

With regard to claim 10, Staplin et al. teach the additional limitation wherein the DMA medium carries out the shift operationg according to the number of bits to be shifted that has a value from 0 to 7 (column 9, lines 50 – 55; Staplin et al. teach that 4 bits (bits 12 – 15) are used when bit 8 equals a binary 0 to determine the number of positions to be shifted. 4 bits would provide a range from 0 to 15).

With regard to claim 11, Tokumaru teaches the additional limitation wherein the DMA medium decides the shift direction and the number of bits to be shifted depends upon bit values (Examiner interprets the shifting signals, which determine the shift direction and number of bits (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) as being part of the DNA medium, and therefore the reference meets this limitation).

* * *

Examiner assumes that the applicant meant to recite classifying the read data, instead of classifying the bit strings configuring the read data in the following:

Claim 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al., and further in view of Beukema et al.

With regard to claim 12, Tokumaru and Staplin et al. teach writing the read data to the second storage medium, but fail to teach the DMA medium classifying the bit

strings configuring the read data into more significant bit strings and less significant bit strings; and rearranging positions of less and more significant bit strings.

Beukema et al. teach the DMA medium classifying bit strings into more significant bit strings and less significant bit strings and rearranging positions of less and more significant bit strings (Figure 6B, 7B, 8; where classifying bit strings and rearranging positions may be interpreted as reflection; column 9, lines 41 – 60; column 16, lines 60 – 67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the method of Beukema into the method of Tokumaru and Staplin et al. This would have been obvious in order to provide DMA transfers on "mixed endian computing systems" in order to promote better performance when converting between the two types of data organization (column 2, lines 38 – 43; column 3, lines 51 – 56).

With regard to claim 13, Beukema et al. teach the additional limitation of wherein the DMA medium rearranges the positions of the less and more significant bit strings when the read data is configured in the form of 32 bits (Figure 4C; column 5, lines 52).

With regard to claim 14, Beukema et al. teach the additional limitation of wherein the DMA medium rearranges the positions of the less and more significant bit strings depends upon bit values (where a bit value may be interpreted as a "reflection bit" (RB); column 9, lines 41 – 58).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
2/15/06